Public

EUV Lithography Insertion

Semicon Taiwan
Taipei

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final

Agenda

- EUV Insertion focus
- EUV Benefits
- Field performance
  - Productivity
  - Imaging, Overlay, Defectivity
- Infrastructure status
- Summary

EUV insertion is focusing on the 7nm node

- EUV insertion is currently focusing on the 7nm node
  - Production 2018, production system shipments 2017
  - Insertion will be determined by the production readiness of EUV versus the complexity of multiple patterning
- EUV initially will replace the most difficult multiple patterning layers
  - Other layers will remain allocated to immersion for the foreseeable future
- DUV and EUV will be available in parallel for many years to come
  - ASML remains committed to advancing both technologies to provide the mix that best meets customers' performance and cost requirements

7nm chip manufactured with EUV system

IBM: "Industry's first 7nm node test chips with functioning transistors"

- Close to 50 percent area scaling improvements over today's most advanced technology
- Scaling, materials and process improvements could result in 50 percent power/performance increase for mainframes, servers

Source: IBM press release, 9 July 2015

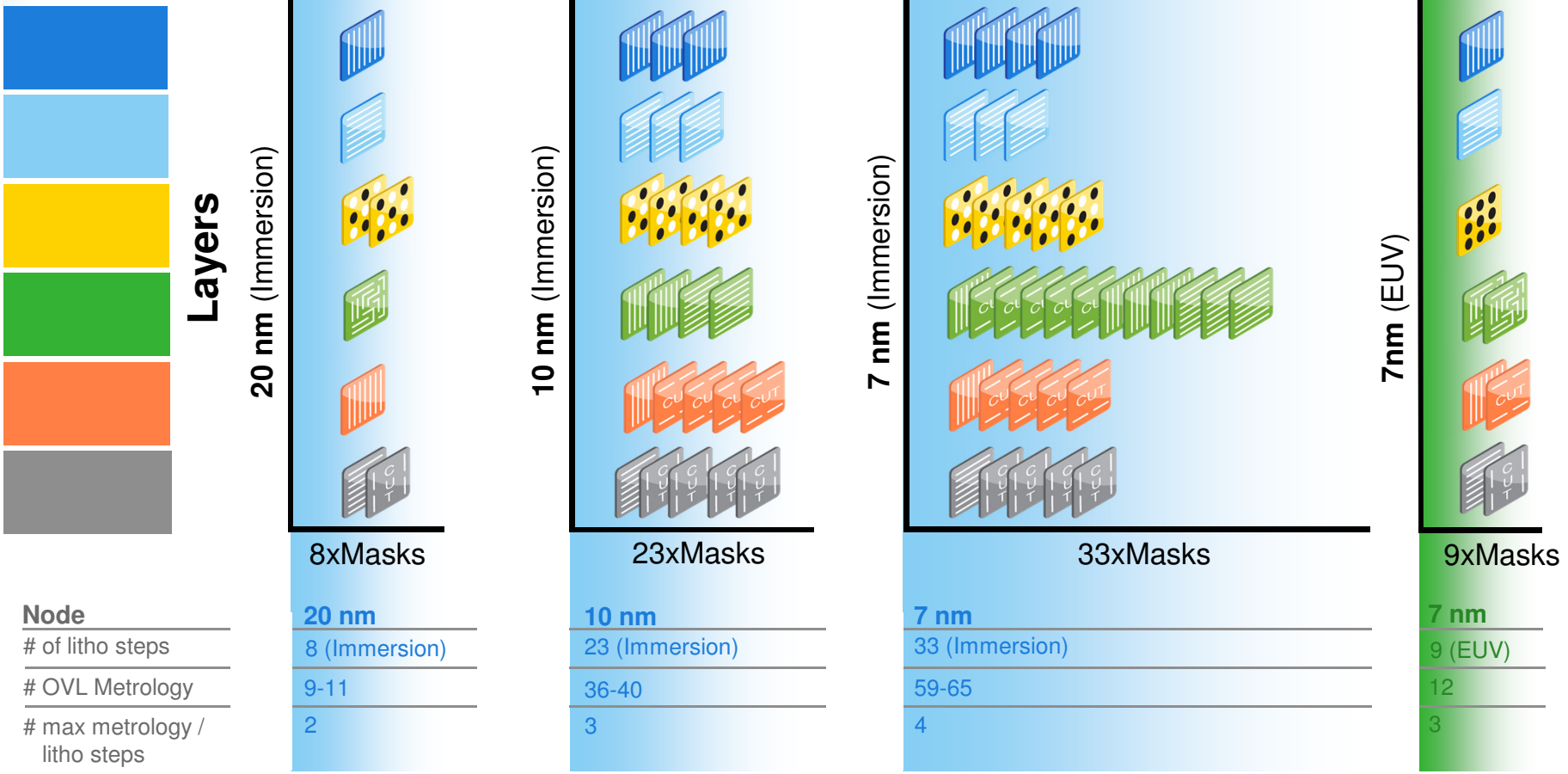
EUV Industrialization Roadmap supports 7nm insertion

By >1500 wafers per day in 2016

Timing	Source power [W]	Throughput [Wafers/hr]	Efficiency* [%]	Productivity [Wafers/day]
2014	80	>55	<50%	>500
2015	125	>75	>50%	>1000
2016	250	>125	>55%	>1500

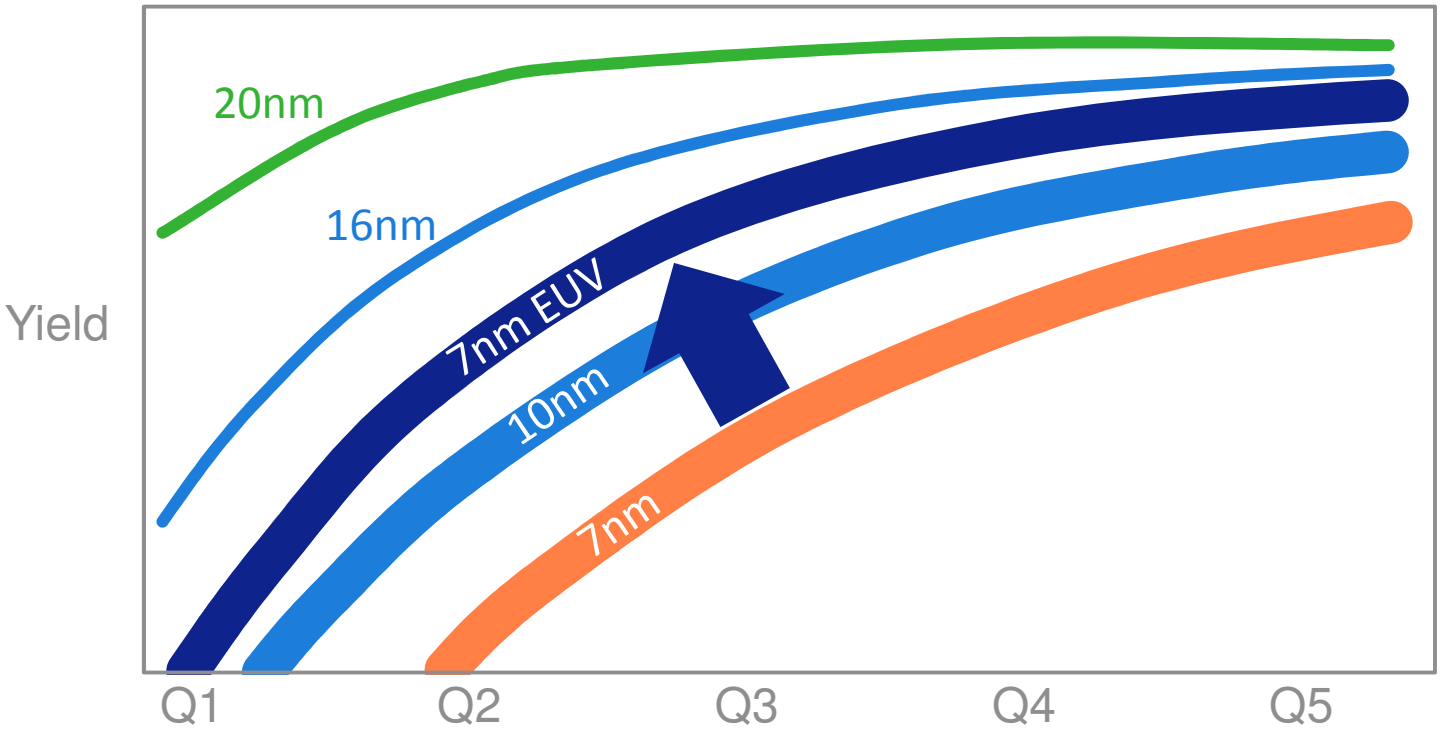
*Efficiency = system availability x customer utilization x customer rate efficiency
Logic typically 55%, for DRAM 70-75% (>2000 WPD)
Illustrative numbers used for WPD model

EUV reduces complexity and thus cycle time



Node	20 nm	10 nm	7 nm	7 nm
# of litho steps	8 (Immersion)	23 (Immersion)	33 (Immersion)	9 (EUV)
# OVL Metrology	9-11	36-40	59-65	12
# max metrology / litho steps	2	3	4	3

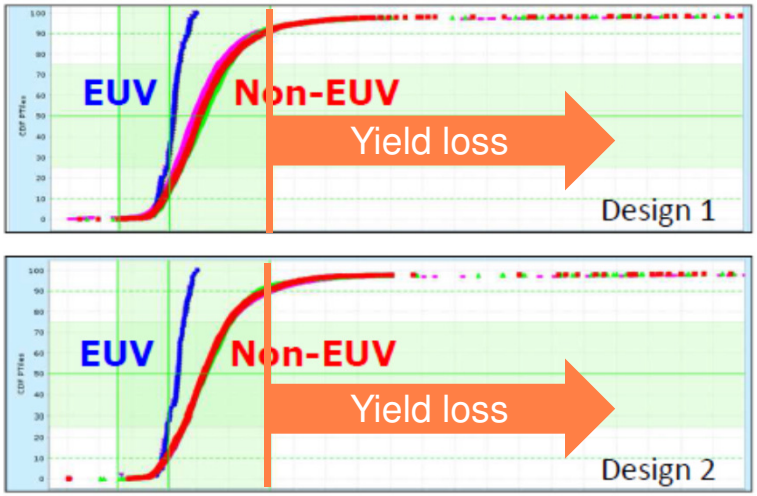
EUV: Reduced complexity enables faster ramp and higher yield



Source: ASML model

EUV improves circuit performance, yield, design flexibility

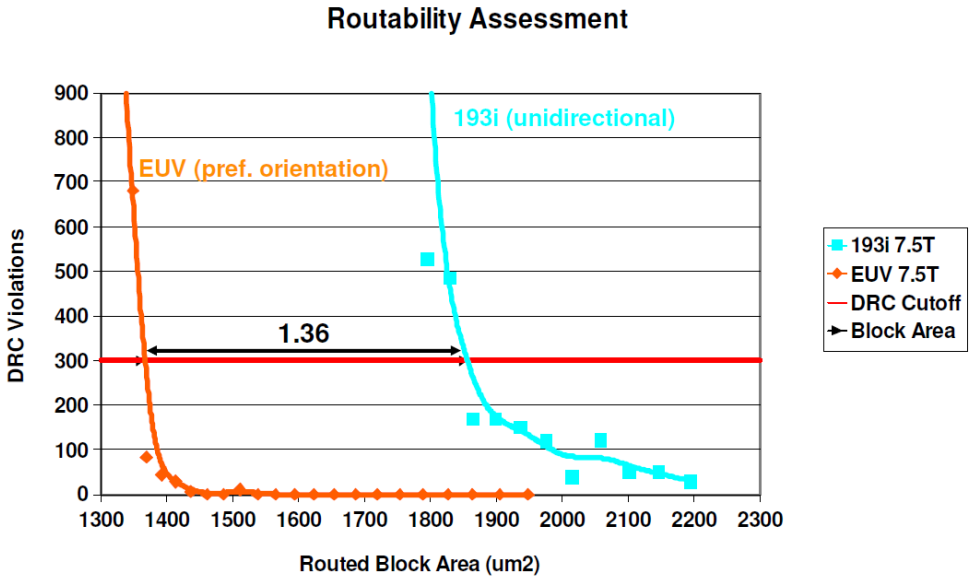
Metal Line Wire Resistance distribution improved with EUV



"In this 10nm node demonstration, EUV wafers with single exposure have tighter distribution compared to optimized multi-patterned 193i lithography"

Source: Jeffrey Shearer et al, IBM, AVS, Nov 2014

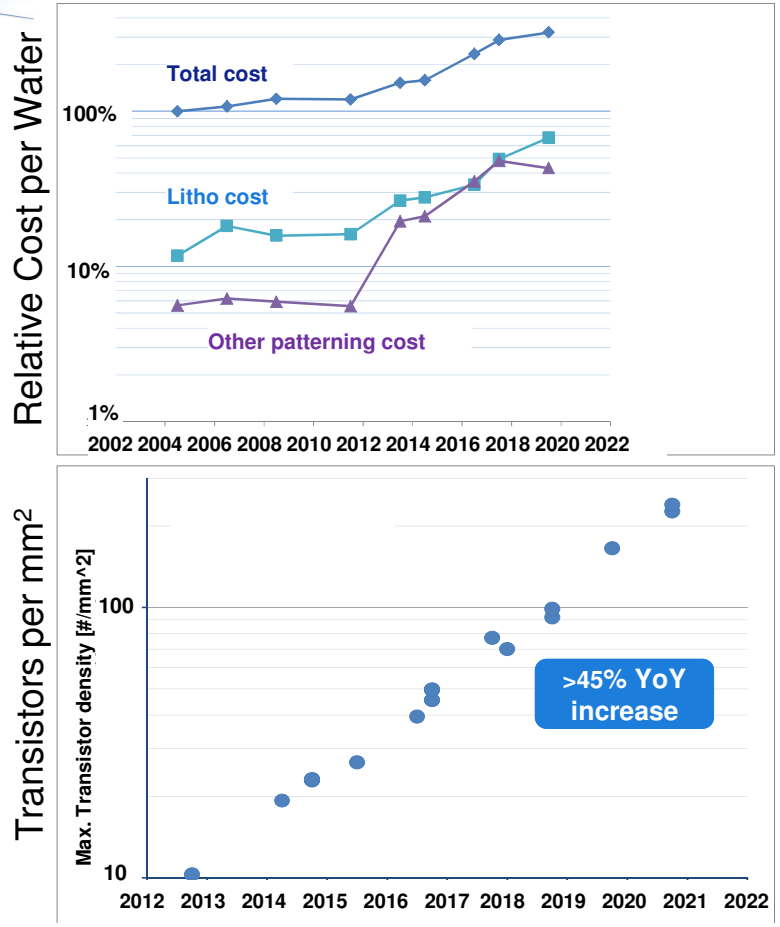
Hard-to-route design can get up to 36% area improvement with EUV

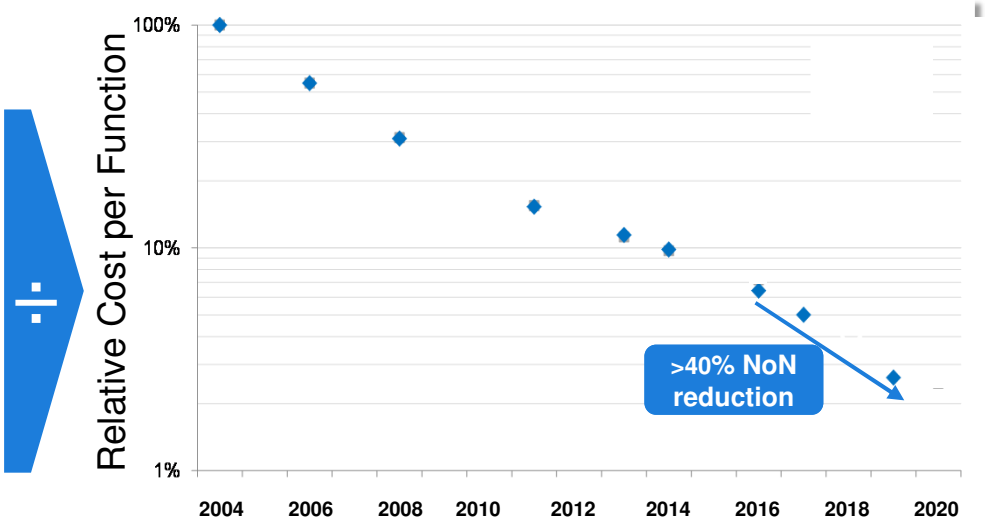


Source: Lars Liebmann et al, IBM, SPIE, Feb 2015

Moore's Law cost reduction stays on track with EUV

Multiple patterning costs reduced





NoN = Node on Node
YoY = Year on Year

Source: ASML, IC Knowledge, IMEC
Validated with external consultants

Source power and availability drive wafers/day

Source power

- All field systems have minimum 40 Watts
- 80 Watt upgrades completed at multiple customer sites
- Dose-controlled 130 Watts demonstrated at ASML

Availability

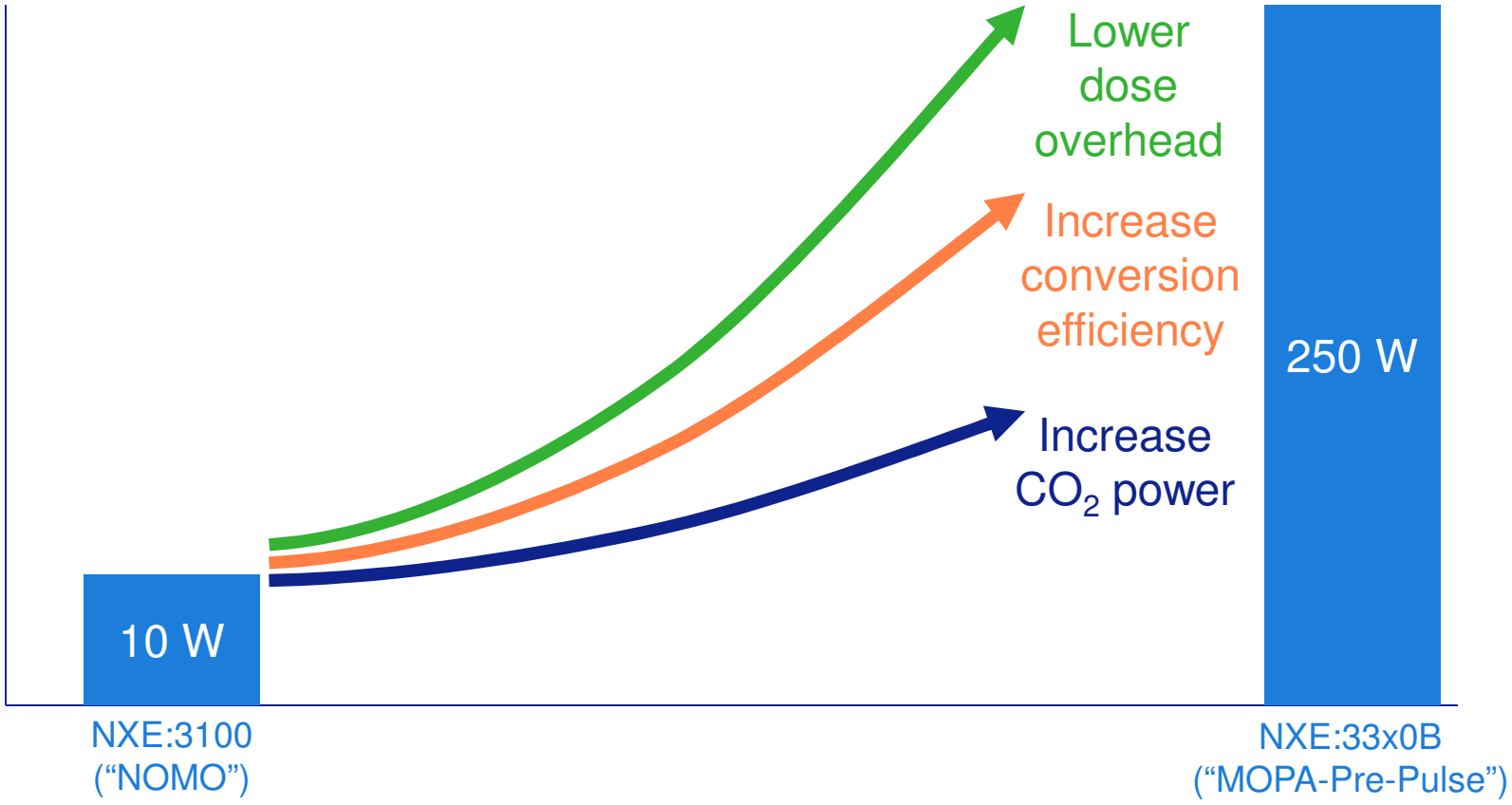
- 55% availability on average for all NXE:3300B sites
- Several sites achieved average availability of >70% for one week
- One customer has achieved a 4-week average availability of 70%
- Availability upgrades being rolled out

Productivity

- Champion data: 1022 wafers/day
- >500 wafers/day achieved on multiple systems, multiple days
- One customer has exposed >500 WpD over 28 consecutive days

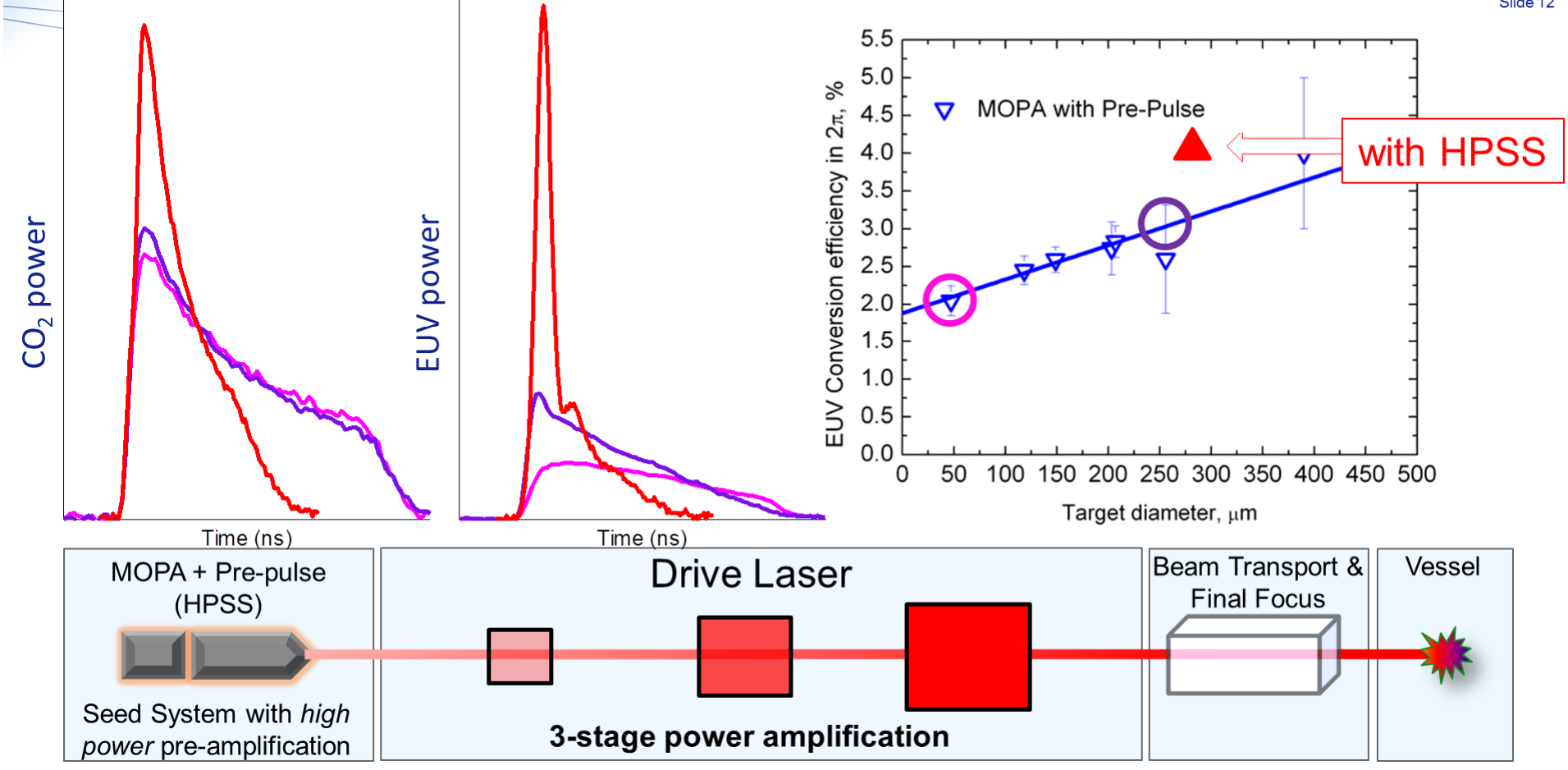
EUV power scaling: three levers

CO_2 power, conversion efficiency, EUV energy available for exposure



EUV power above 100W by improved conversion efficiency

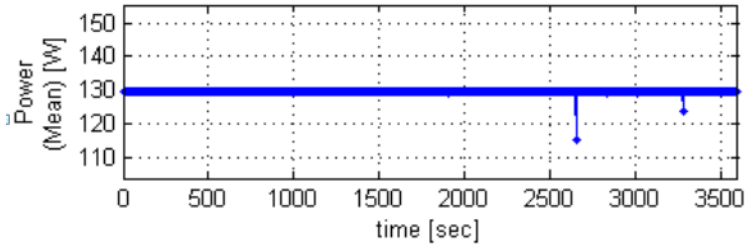
High Power Seed System drives up conversion efficiency by higher CO_2 peak power



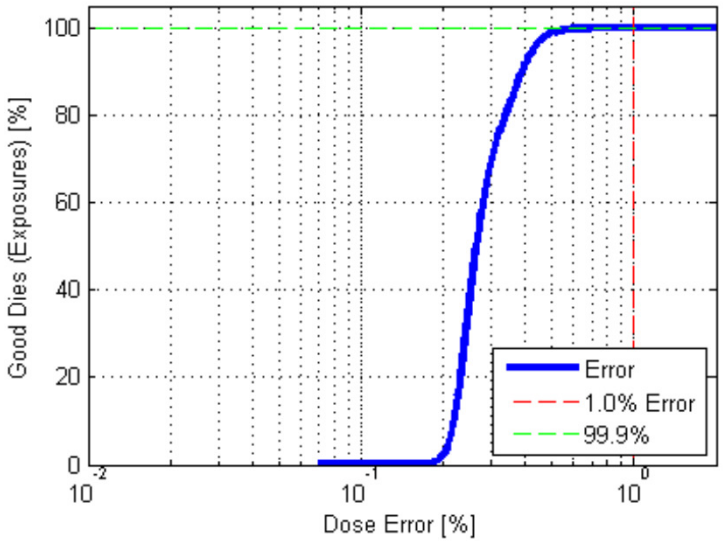
130 Watt dose-controlled EUV power shown at ASML

With high-power CO_2 system

Power

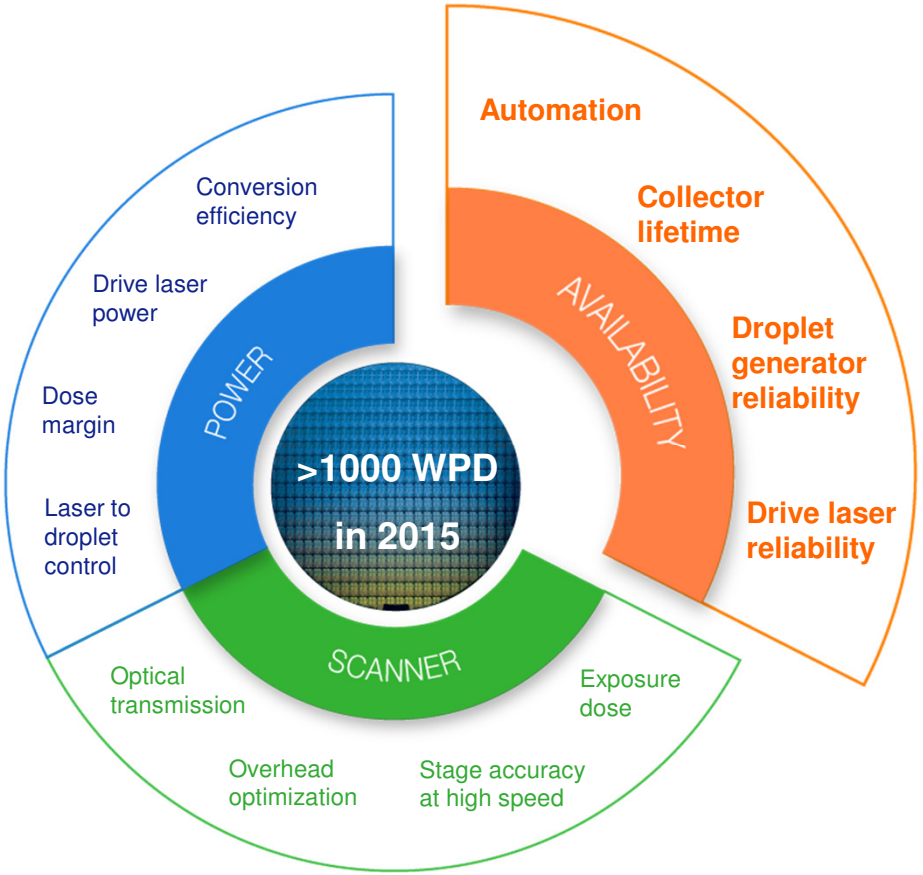


Exposures



Focus 2015: improving source availability

More than 50 improvement items identified, field upgrades throughout 2015

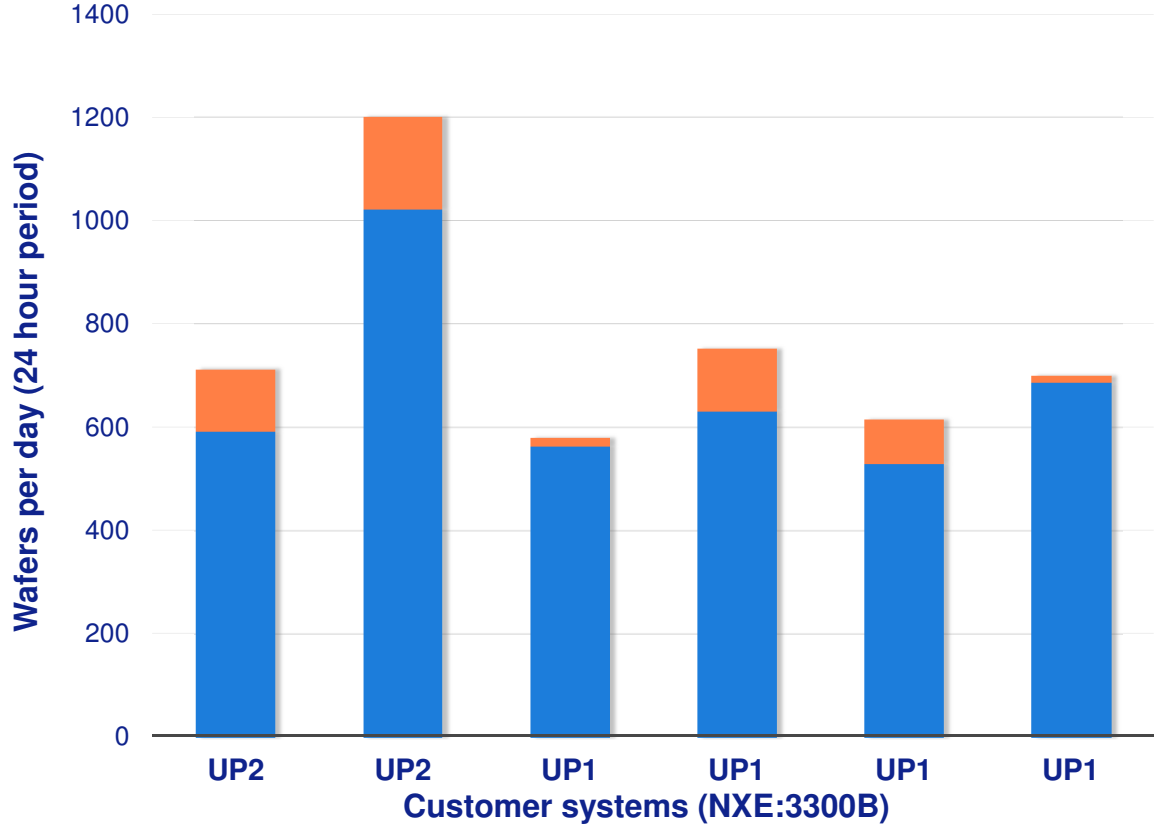


More than 50 availability improvement items have been identified.

Projects are underway to make these improvements available on customer systems throughout this year.

2015 target >1000 wafers/day proven at 80W

Capability > 1200 wafers per day at maximum utilization shown



Maximum number of customer wafer exposures in a 24 hour period

Configuration:

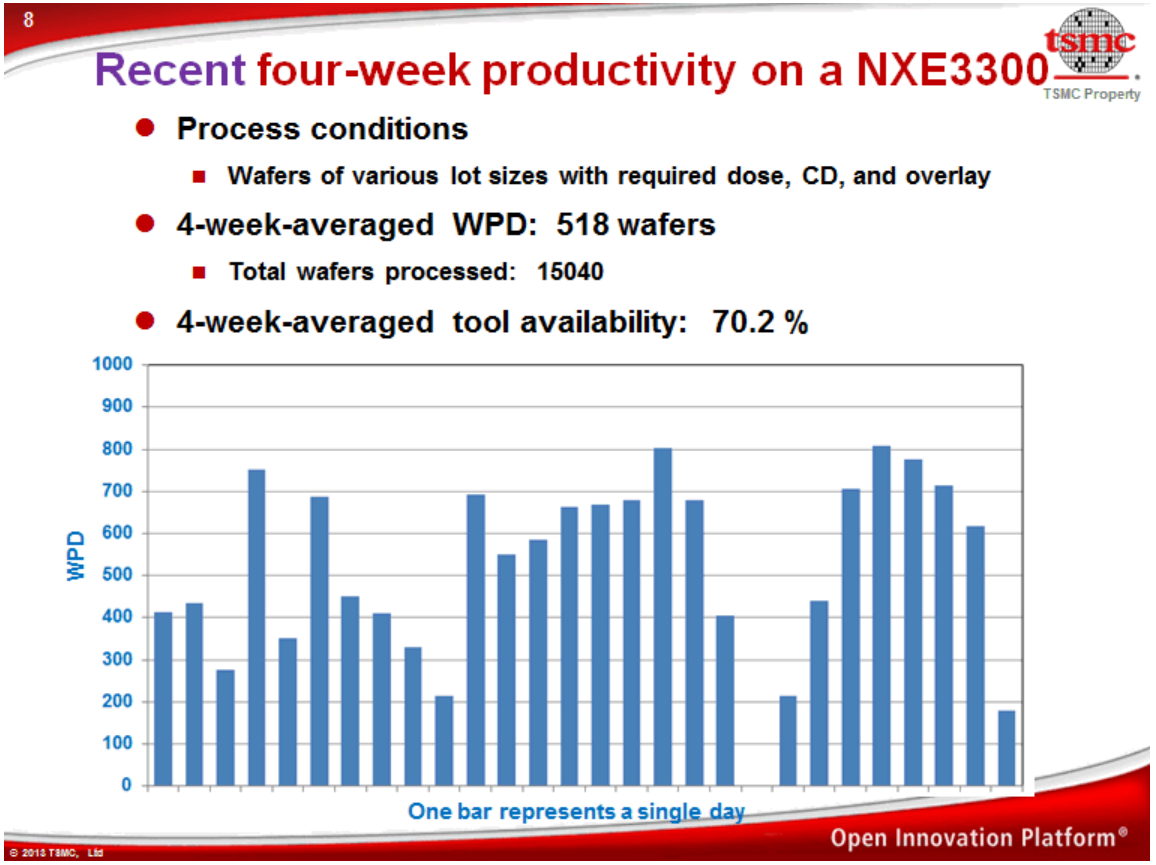
- NXE:3300B
- EUV Source:
  - UP2: 80 Watts configuration
  - UP1: 40 Watts configuration
- Customer exposure recipes

Actual customer exposures

Customer exposures at 100% utilization

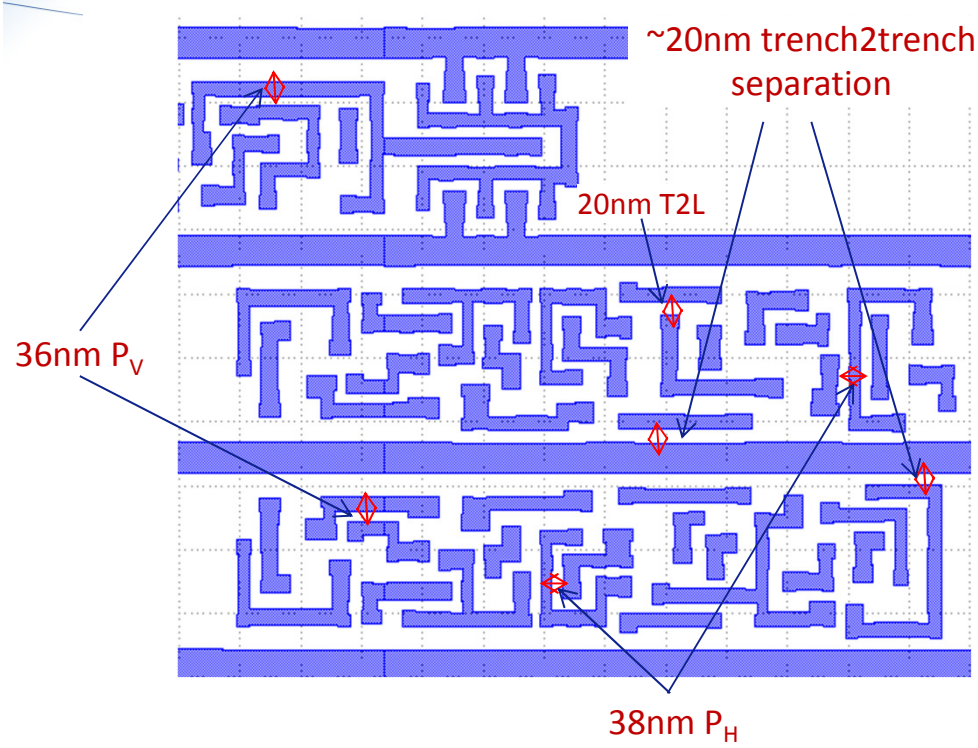
> 500WPD in 4 consecutive weeks proven at customer

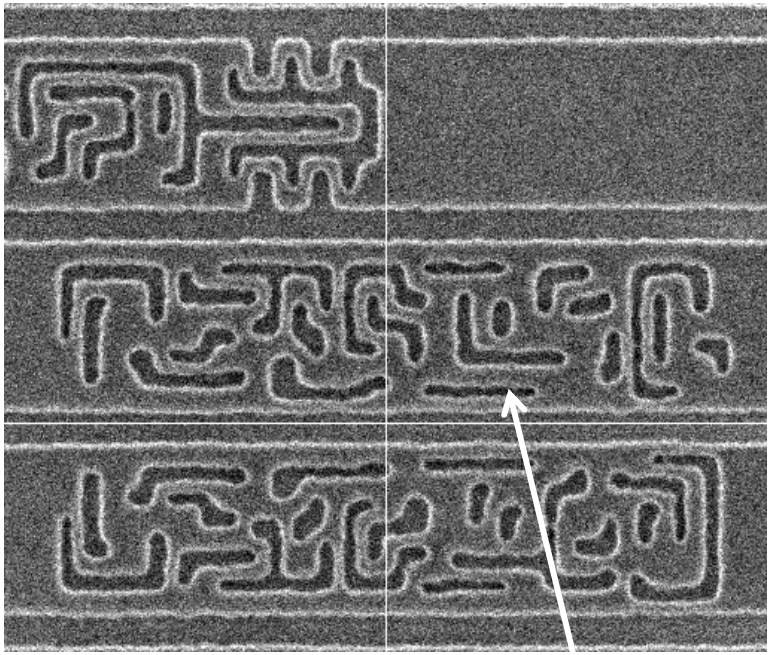
Automated reticle & wafer loading. Imaging & overlay in specification



7nm Logic clip imaged with good fidelity

Routed 2D semi-gridded Metal, 36x38nm (P_V x P_H)





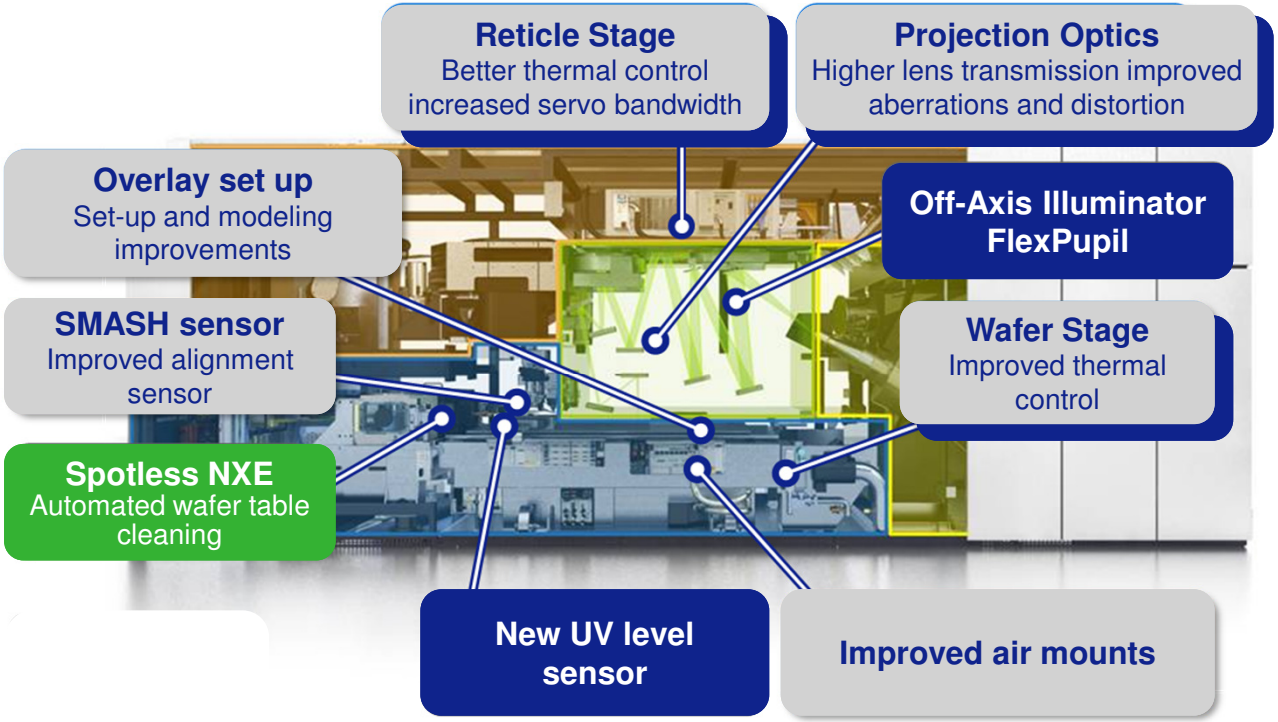
This example would require 4 exposures with 193 immersion – or one with 0.33NA EUVL

Conditions: NXE:3300B, quasar illumination, 60nm resist, 40mJ/cm^2 dose

imec

NXE:3350B Supports 7nm logic insertion

by strongly improved overlay and resolution



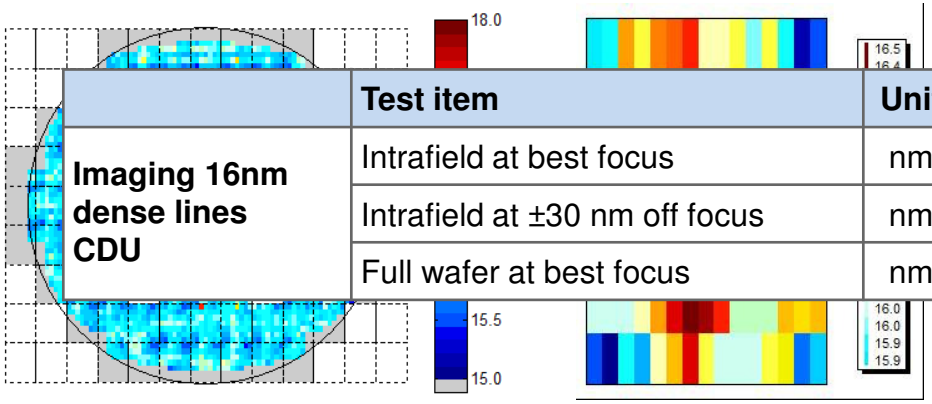
Resolution	16nm
Full wafer CDU	≤ 1.3nm
DCO	≤ 1.5nm
MMO	≤ 2.5nm
Focus control	≤ 70nm
Productivity	≥ 125 WPH

Overlay
Imaging/Focus
Productivity

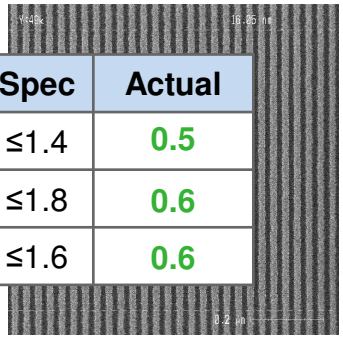
NXE:3350 Imaging meets 7nm requirements

16nm dense lines and 20nm iso space: 0.6nm Full Wafer CDU, 0.4nm intra-field

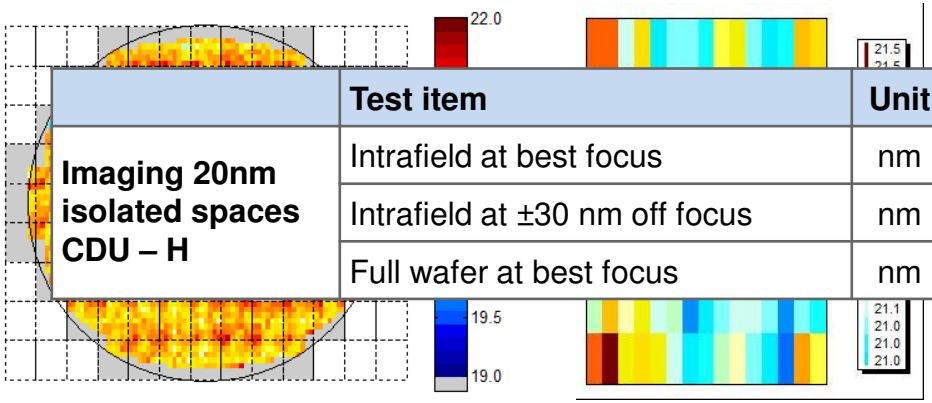
16nm dense lines



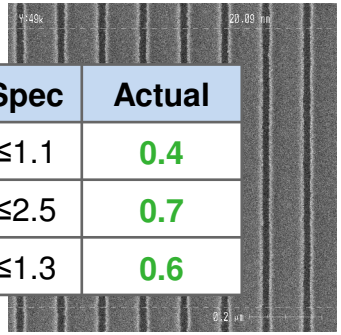
	Test item	Unit	Spec	Actual
Imaging 16nm dense lines CDU	Intrafield at best focus	nm	≤1.4	**0.5**
	Intrafield at ±30 nm off focus	nm	≤1.8	**0.6**
	Full wafer at best focus	nm	≤1.6	**0.6**



20nm iso space



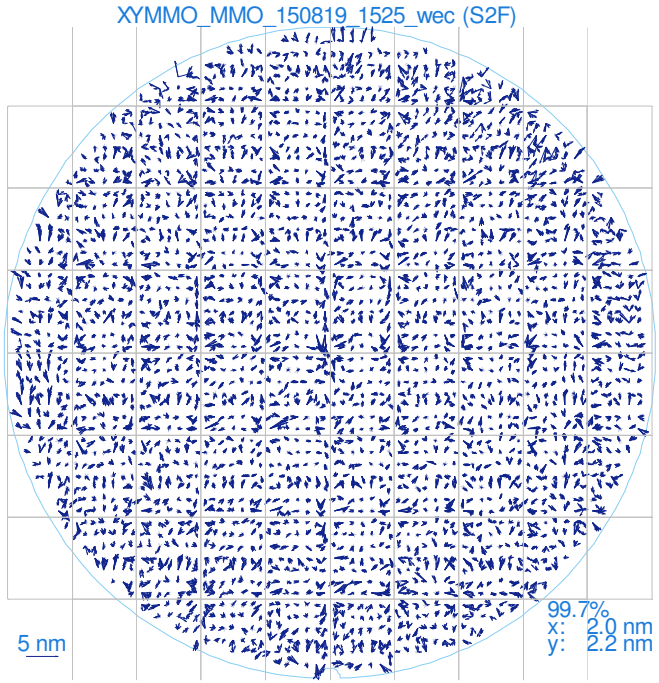
	Test item	Unit	Spec	Actual
Imaging 20nm isolated spaces CDU – H	Intrafield at best focus	nm	≤1.1	**0.4**
	Intrafield at ±30 nm off focus	nm	≤2.5	**0.7**
	Full wafer at best focus	nm	≤1.3	**0.6**

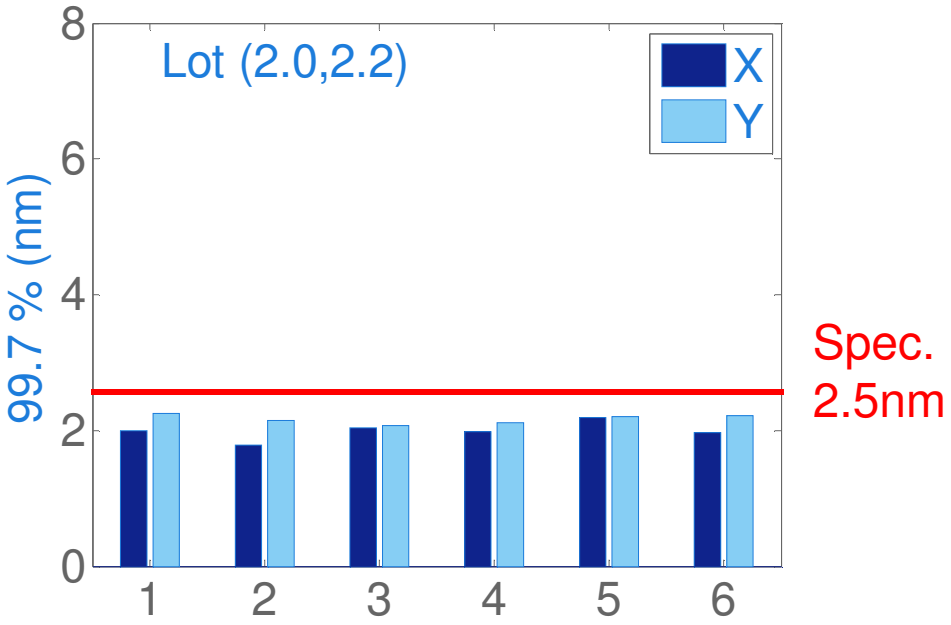


Tested with new ATP – 0mm field spacing and 15x9 grid

NXE:3350 Matched Machine Overlay: 2.2nm

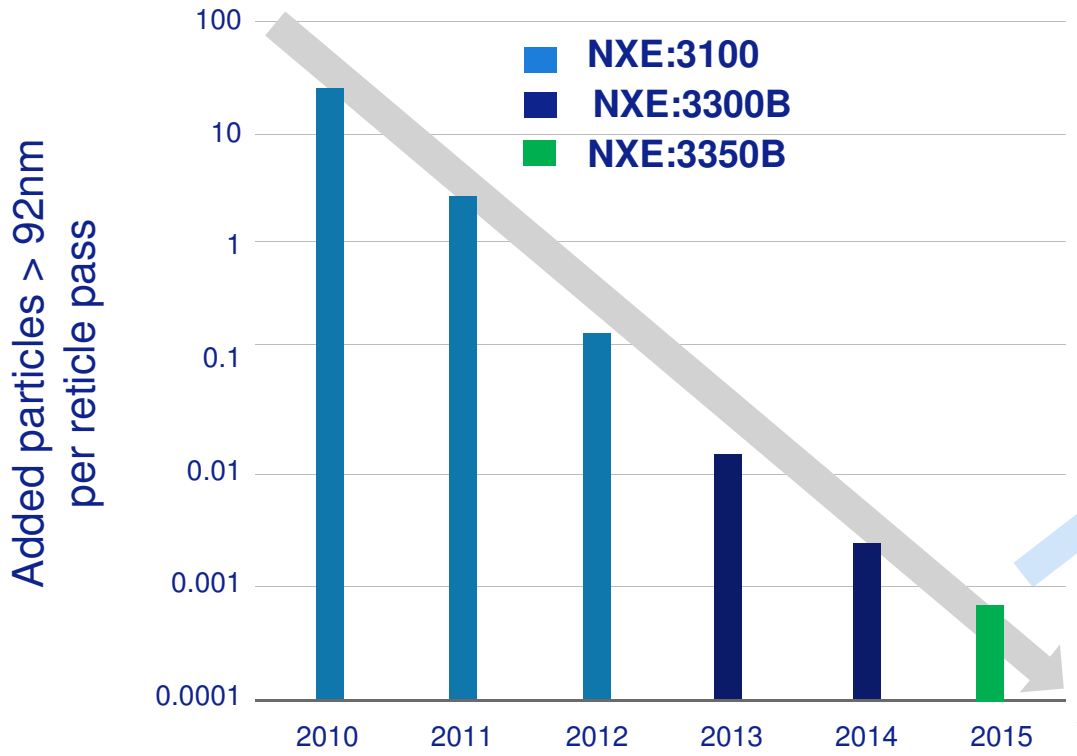
Full wafer, matched to Baseliner MMO wafers, Wafer Error Correction applied





Spec.
2.5nm

Front-side reticle defectivity: 10x reduction/year realized

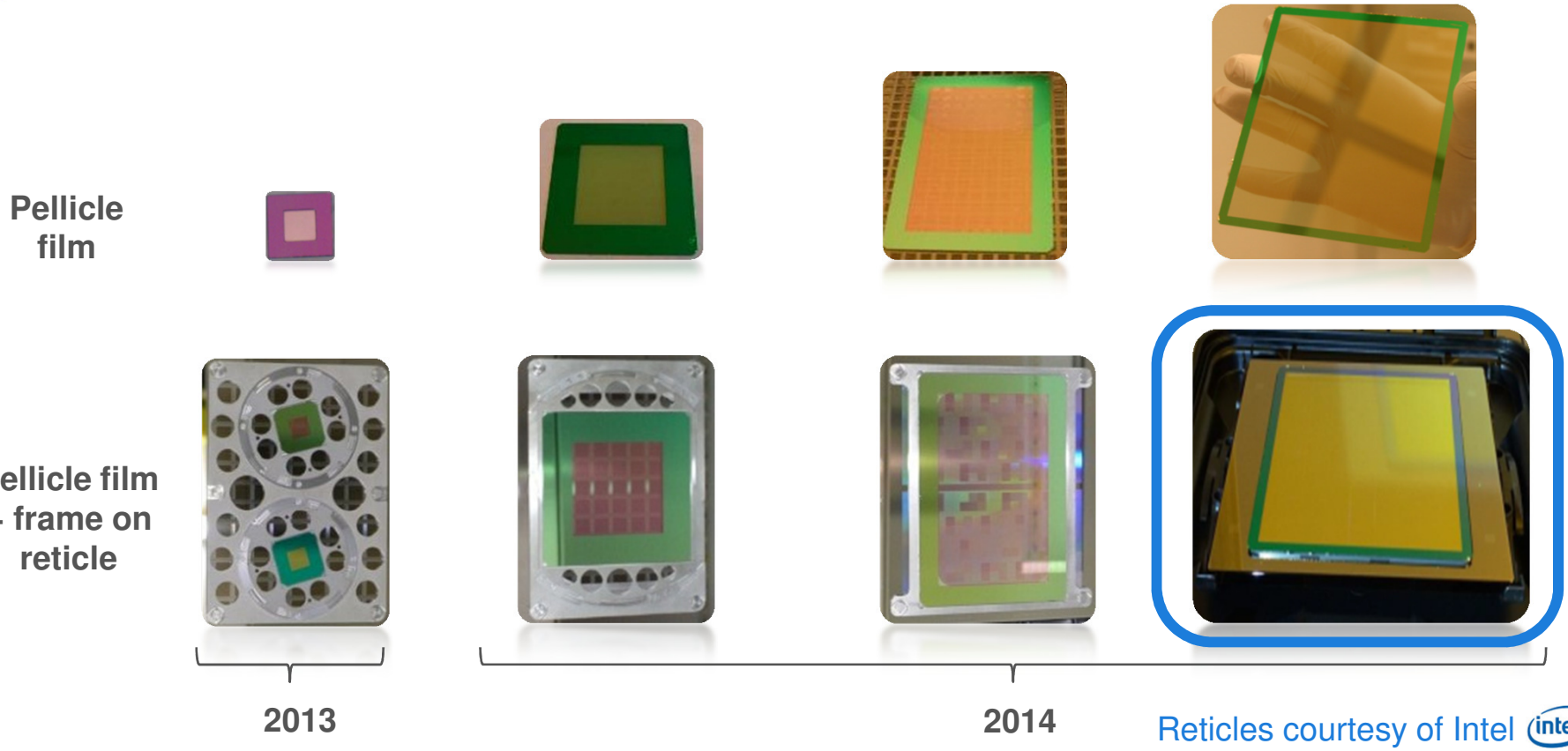


Test	# Cycles	# Added Particles	PRP Value
A	228	0	< 0.004
B	140	0	< 0.007
C	450	0	< 0.002
D	222	1	0.0045
E	133	0	< 0.007
Cumulative	**1173**	**1**	**0.0008**

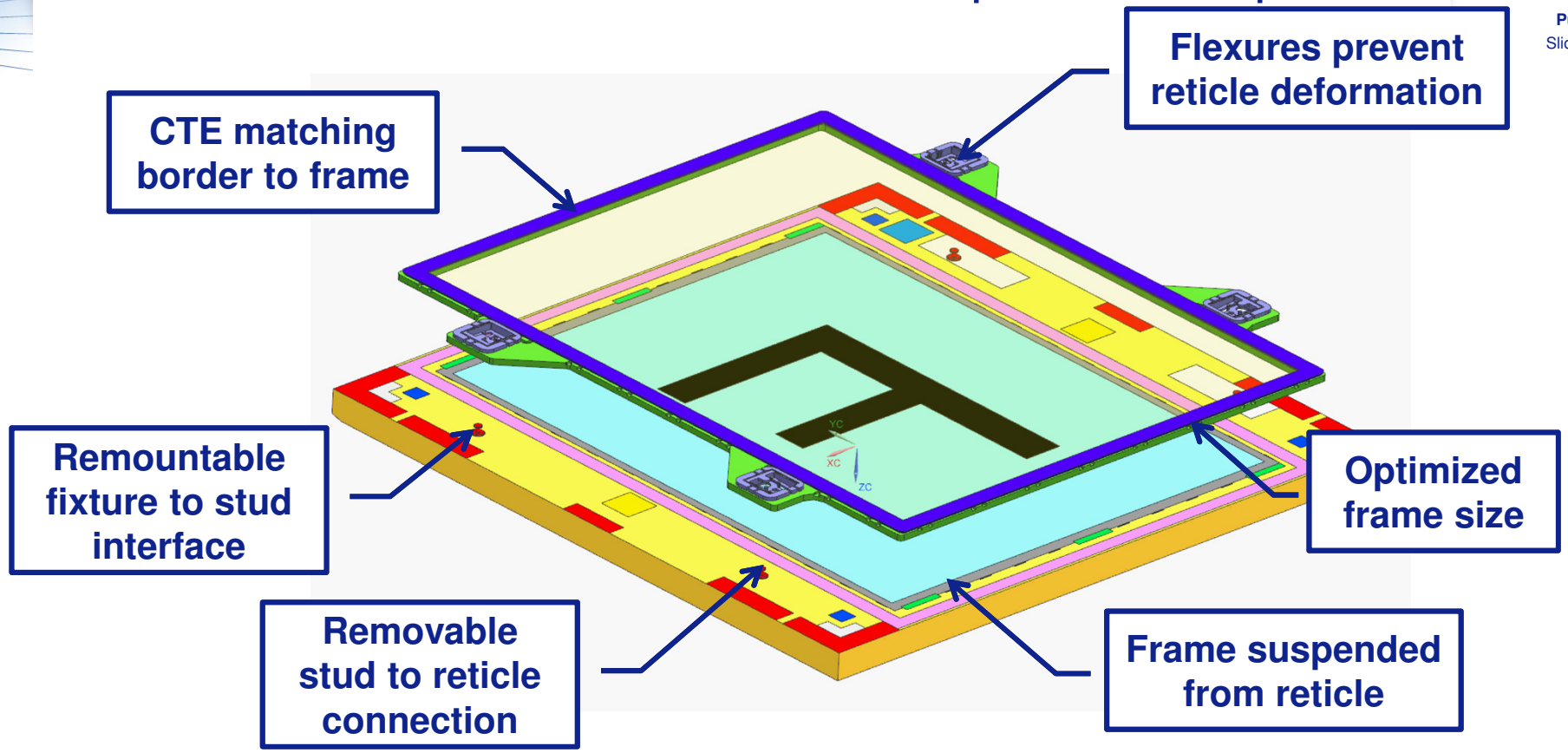
Customer requirement for full production without pellicle

EUV pellicle films successfully tested in ASML EUV tools

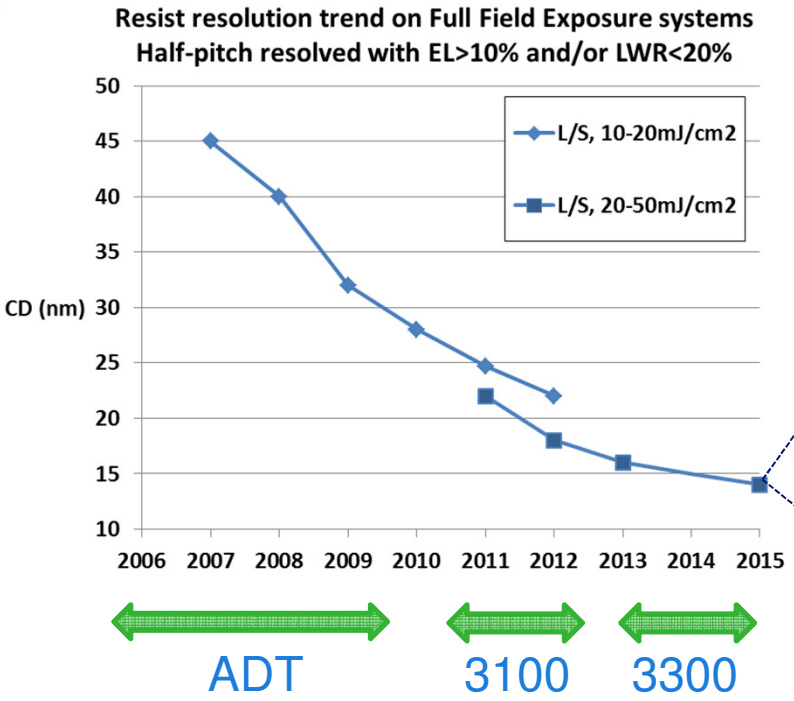
Mechanical compatibility and imaging performance of pellicle film demonstrated

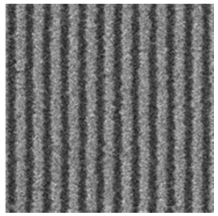


Removable NXE Pellicle frame concept in development



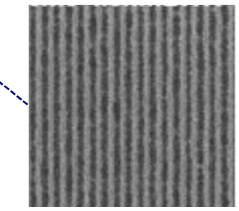
Photoresist approaching 7nm requirements





13.5nm V L/S

13nm HP resolution with CAR
dose to size 31.5 mJ/cm^2
LWR < 2.7nm



13nm V L/S

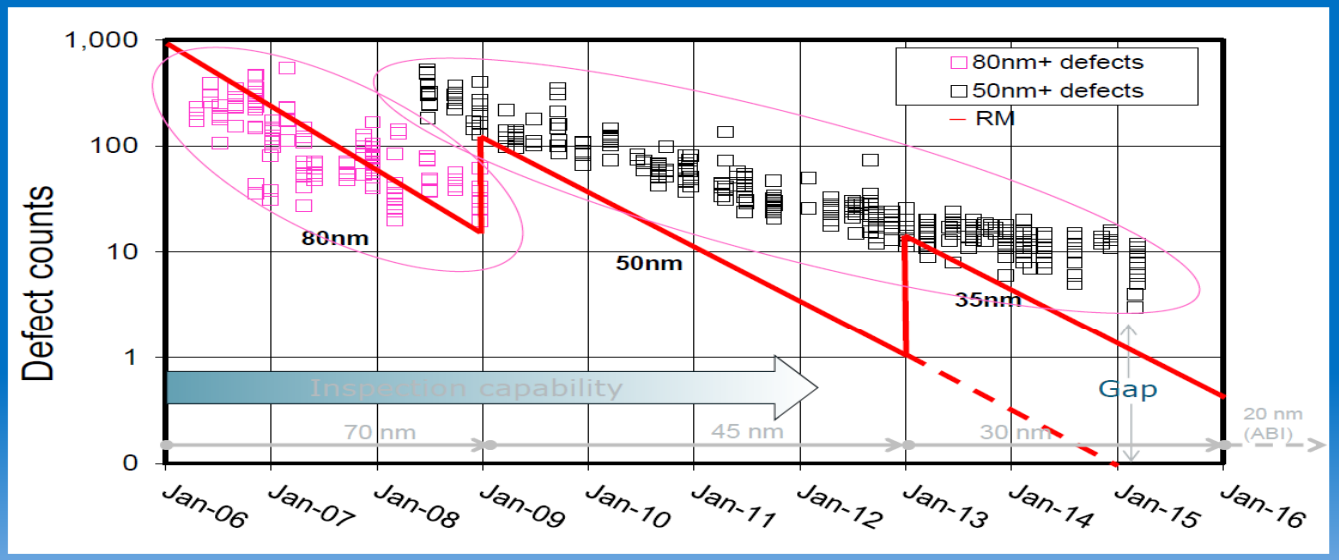
13nm HP resolution with non-CAR
dose to size 35 mJ/cm^2
LWR < 2.6nm

ADT, NXE:3100, NXE:3300 as measured by ASML/ IMEC

CAR: chemically amplified resist

EUV mask blank defect density is steadily improving

EUV mask blank ML defect trend



- EUV blanks with single digit (ML) defect count at 50 nm become commercially available
- Gap to the RM still needs to be closed for HVM
- Advanced inspection capability is required for further defect reduction

EUV Insertion: “WHEN” not “IF”

- Customers differ in exactly “WHEN” EUV will go to volume production
  - EUV insertion is focusing on the 7nm node
  - Production 2018, production system shipments 2017
- EUV is making continued progress on the Wafers-per-Day roadmap
  - >500WpD at multiple customers
  - >500WpD over 4 consecutive weeks shown at one customer
  - Roadmap in place to deliver 1500 WpD in 2016 for 7nm insertion
  - Continued focus on availability to >90%
- EUV imaging & overlay meeting 7nm node requirements
- EUV infrastructure progressing towards 7nm volume production


ASML